INTRODUCTORY COMMENT:

Most active electronic devices are based on transistors as the fundamental amplifying component. However, in this era, very little electronic circuit design is done using isolated transistors. Rather, integrated devices, such as the op-amps that you have just studied, are the building blocks from which circuits are constructed. This lab on transistors is intended to help you develop some understanding of the characteristics of the fundamental amplifying units.

There are two types of transistors. Field-effect transistors (JFETs and MOSFETs) are high-input-impedance devices, while bipolar junction transistors (BJTs) are low-input-impedance devices. This lab deals with JFETs, which may be easier to conceptualize, and with BJTs.

LEARNING OBJECTIVES:

(1) To become familiar with the basic properties of JFETs, particularly as used in a simple amplifier application.

(2) To gain further practice in wiring devices into circuits and in measuring amplifier characteristics.

(3) To become familiar with the basic properties of BJTs used as a simple amplifier and as a constant current source.

REFERENCES:


L.R. Fortney, Principles of Electronics, Analogue and Digital, Chapter 6.

WHAT TO DO:

NOTE: Use the same FET (2N3819 general purpose n-channel FET) for all parts 1, 2, and 3.

(1) Using the circuit in the figure below with a 2N3819 JFET, plot \( (I_D)^{1/2} \) vs. \( V_{GS} \) by varying the value of the source bias resistor \( R \). (\( R \) could be one of the larger 10 k\( \Omega \) “pots” or a resistance box.) Before proceeding on with the experiment, deduce from your graph the best fit values of \( V_P \) and \( I_{DSS} \) in the equation:

\[
I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2.
\]

Note that \( V_P \) (the pinch-off voltage) and \( I_{DSS} \) (the drain to source current when the gate is shorted to the source) are constants of the particular JFET that you are using. \( V_P \) is negative for n-channel JFETs.

(2) Using the circuit in the figure below, with the same 2N3819 JFET, adjust \( R_S \) to make the drain current \( I_D = 0.5 \) mA. Measure the gain of the circuit at 10 kHz and find the maximum undistorted output voltage. Verify that the gain of the circuit approximately agrees with the formula:

\[
A = -g_m R_L \quad \text{where} \quad g_m = 2 \sqrt{\frac{I_{DSS}}{V_P}}.
\]

Note that \( V_P \) and \( I_{DSS} \) are constant characteristics of your particular device, while \( I_D \) is your own imposed operating current.
(3) Repeat the measurement of part (2), but with the source bypass capacitor, $C_S$ removed from the circuit. Is the gain equal to the ratio $R_L/R_S$? Negative feedback is operating in this case. Explain how.

(4) Using the circuit in the following figure with a 2N3904 BJT, measure the small signal gain at 10 kHz and verify that its value is $-g_m \times R_L$, where $g_m = 40 \times I_C$ ($g_m$ in $\Omega^{-1}$, $I_C$ in Amperes).

(5) Using the same 2N3904 BJT as in part (4), but modifying the circuit by removing the input capacitor and $C_E$, the emitter bypass capacitor (as shown in the circuit below), you may now consider this new circuit as a constant current source feeding the collector load resistor $R_L$. Test out the constancy of this source (or in other words, measure the circuit impedance). Do this measurement at DC (by observing the voltage across $R_L$ as you vary $R_L$) and also do the measurement at 1 kHz by putting a voltage source in series with $R_L$ and measuring the voltage drop across $R_L$ using the differential voltage capability of your CRO.

**COMMENTS:**

At each step in this experiment, be sure that you understand what you see and explain in your lab notebook how the circuits are operating. In your analysis, be sure that you understand and explain the roles of all the capacitors in the circuits.